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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,301	07/28/2003	Lewis B. Aronson	15436.247.2.1.3	6453

22913 7590 04/01/2008

WORKMAN NYDEGGER
60 EAST SOUTH TEMPLE
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EXAMINER	
PHAN, HANH	
ART UNIT	**PAPER NUMBER**
2613	
MAIL DATE	**DELIVERY MODE**
04/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/629,301	ARONSON ET AL.	
	Examiner	Art Unit	
	Hanh Phan	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 01/09/2008.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-8, 10-27 and 29-38 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 7,099,382 (Aronson et al) in view of Marmur (US Patent No. 6,832,052).

10/629,301 (Claim 1)	US Patent No. 7,099,382 (Claim 1)
An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data	An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data

stream;	stream (Claim 1);
receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;	receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream (Claim 1);
a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;	a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (Claim 1);
receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream;	
a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;	a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit (Claim 1);
transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and	transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream (Claim 1); and
a second electrical output port for	a second electrical output port for

transmitting the retimed and reshaped second serial electrical data stream.	transmitting the retimed and reshaped second serial electrical data stream (Claim 1).

Aronson et al differs from claim 1 in that he does not disclose receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream. However, Marmur discloses receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (i.e., Figures 1 and 2, col. 2, lines 45-67 and col. 3, lines 1-46). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream as taught by Marmur in the system of Aronson et al. One of ordinary skill in the art would have been motivated to do this since allowing performance monitoring of optical signals of different transmission protocols at one or more different bit rates.

Regarding claim 2, the combination of Aronson et al and Marmur teaches wherein the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data

rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 3, the combination of Aronson et al and Marmur teaches the receiver eye opener circuitry has a data rata range including 10 Gb/s; and the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 4, the combination of Aronson et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 5-7, 14, 15, the combination of Aronson et al and Marmur teaches the bypass data path is selected in response to a loss of lock (LOL) signal or a loss of signal (LOS) signal or a command received from external to the integrated circuit (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 8, the combination of Aronson et al and Marmur teaches bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 10, 21, the combination of Aronson et al and Marmur teaches power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., see claim 6 of Aronson et al).

Regarding claims 11, 16-20 and 22-38, Similarly as described above, the combination of Aronson et al and Marmur teaches an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and transmitting the retimed and reshaped second serial electrical data stream (i.e., see claim 1 of Aronson et al and see Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 12, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a

predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 13, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

4. Claims 9 and 28 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 7,099,382 (Aronson et al) in view of Marmur (US Patent No. 6,832,052) and further in view of Jiang et al (US Patent No. 6,665,498).

Regarding claims 9 and 28, the combination of Aronson et al and Marmur differs from claims 9 and 28 in that it fails to teach an adaptive equalizer. However, Jiang et al teaches an equalizer (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the equalizer as taught by Jiang et al in the system of the combination of Aronson et al and Marmur. One of ordinary skill in the art would have been motivated to do this since allowing reducing the distortion of the signal and reducing the noise signal and error signal.

5. Claims 1-8, 10-27 and 29-38 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3,

Application/Control Number: 10/629,301
Art Unit : 2613
5-14, 16 and 18-22 of Copending Application No. 10/420,027 (Aronson et al) in view of Marmur (US Patent No. 6,832,052).

10/629,301 (Claim 1)	Copending Appication No. 10/420,027 (Claim 1)
An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream;	An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream (Claim 1);
receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;	receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream (Claim 1);
a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;	a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (Claim 1);
receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream;	
a second electrical input port for	a second electrical input port for

receiving a second serial electrical data stream from external to the integrated circuit;	receiving a second serial electrical data stream from external to the integrated circuit (Claim 1);
transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and	transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream (Claim 1); and
a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.	a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream (Claim 1).

Aronson et al differs from claim 1 in that he does not disclose receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream. However, Marmur discloses receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (i.e., Figures 1 and 2, col. 2, lines 45-67 and col. 3, lines 1-46). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but

bypassing retiming and reshaping of the first serial electrical data stream as taught by Marmur in the system of Aronson et al. One of ordinary skill in the art would have been motivated to do this since allowing performance monitoring of optical signals of different transmission protocols at one or more different bit rates.

Regarding claim 2, the combination of Aronson et al and Marmur teaches wherein the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 3, the combination of Aronson et al and Marmur teaches the receiver eye opener circuitry has a data rata range including 10 Gb/s; and the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 4, the combination of Aronson et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 5-7, 14 and 15, the combination of Aronson et al and Marmur teaches the bypass data path is selected in response to a loss of lock (LOL) signal or a loss of signal (LOS) signal or a command received from external to the integrated circuit (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 8, the combination of Aronson et al and Marmur teaches bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 10 and 21, the combination of Aronson et al and Marmur teaches power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., see claim 1 of Aronson et al).

Regarding claims 11, 16-20 and 22-38, Similarly as described above, the combination of Aronson et al and Marmur teaches an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and transmitting the retimed and reshaped second serial electrical data stream (i.e., see claim 1 of Aronson et al and see Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 12, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 13, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

This is a provisional obviousness-type double patenting rejection.

6. Claims 9 and 28 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, 5-14, 16 and 18-22 of Copending Application No. 10/420,027 (Aronson et al) in view of Marmur (US Patent No. 6,832,052) and further in view of Jiang et al (US Patent No. 6,665,498).

Regarding claims 9 and 28, the combination of Aronson et al and Marmur differs from claims 9 and 28 in that it fails to teach an adaptive equalizer. However, Jiang et al teaches an equalizer (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-

48). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the equalizer as taught by Jiang et al in the system of the combination of Aronson et al and Marmur. One of ordinary skill in the art would have been motivated to do this since allowing reducing the distortion of the signal and reducing the noise signal and error signal.

This is a provisional obviousness-type double patenting rejection.

7. Claims 1-38 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5, 8-24 and 27-32 of Copending Application No. 10/629,228 (Aronson et al) in view of Marmur (US Patent No. 6,832,052).

10/629,301 (Claim 1)	Copending Application No. 10/629,228 (Claim 1)
An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream;	An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream (Claim 1);
receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;	receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream (Claim 1);
a first electrical output port for transmitting the retimed and reshaped first	a first electrical output port for transmitting the retimed and reshaped first

serial electrical data stream to external to the integrated circuit;	serial electrical data stream to external to the integrated circuit (Claim 1);
receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream;	
a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;	a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit (Claim 1);
transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and	transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream (Claim 1); and
a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.	a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream (Claim 1).

Aronson et al differs from claim 1 in that he does not disclose receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream. However, Marmur discloses receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (i.e., Figures 1 and 2, col. 2, lines 45-67 and col. 3, lines 1-46). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream as taught by Marmur in the system of Aronson et al. One of ordinary skill in the art would have been motivated to do this since allowing performance monitoring of optical signals of different transmission protocols at one or more different bit rates.

Regarding claim 2, the combination of Aronson et al and Marmur teaches wherein the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 3, the combination of Aronson et al and Marmur teaches the receiver eye opener circuitry has a data rata range including 10 Gb/s; and the bypass data path is selected when the first serial electrical data stream has a data

rate below approximately 3 Gb/s (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 4, the combination of Aronson et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 5-7, 14 and 15, the combination of Aronson et al and Marmur teaches the bypass data path is selected in response to a loss of lock (LOL) signal or a loss of signal (LOS) signal or a command received from external to the integrated circuit (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 8, the combination of Aronson et al and Marmur teaches bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 9 and 28, the combination of Aronson et al and Marmur teaches an adaptive equalizer (i.e., see claim 1 of aronson et al).

Regarding claims 10 and 21, the combination of Aronson et al and Marmur teaches power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., see claim 6 of Aronson et al).

Regarding claims 11, 16-20 and 22-38, Similarly as described above, the combination of Aronson et al and Marmur teaches an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and transmitting the retimed and reshaped second serial electrical data stream (i.e., see claim 1 of Aronson et al and see Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 12, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 13, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the

bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

This is a provisional obviousness-type double patenting rejection.

8. Claims 1-8, 10-27 and 29-38 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-26 of Copending Application No. 10/629,302 (Aronson et al) in view of Marmur (US Patent No. 6,832,052).

10/629,301 (Claim 1)	Copending Application No. 10/629,302 (Claim 1)
An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream;	An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream (Claim 1);
receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;	receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream (Claim 1);
a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;	a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (Claim 1);

receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream;	
a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;	a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit (Claim 1);
transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and	transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream (Claim 1); and
a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.	a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream (Claim 1).

Aronson et al differs from claim 1 in that he does not disclose receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial

electrical data stream. However, Marmur discloses receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (i.e., Figures 1 and 2, col. 2, lines 45-67 and col. 3, lines 1-46). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream as taught by Marmur in the system of Aronson et al. One of ordinary skill in the art would have been motivated to do this since allowing performance monitoring of optical signals of different transmission protocols at one or more different bit rates.

Regarding claim 2, the combination of Aronson et al and Marmur teaches wherein the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 3, the combination of Aronson et al and Marmur teaches the receiver eye opener circuitry has a data rata range including 10 Gb/s; and the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 4, the combination of Aronson et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has a data rate

that is not within a data rate range of the receiver eye opener circuitry (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 5-7, 14 and 15, the combination of Aronson et al and Marmur teaches the bypass data path is selected in response to a loss of lock (LOL) signal or a loss of signal (LOS) signal or a command received from external to the integrated circuit (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 8, the combination of Aronson et al and Marmur teaches bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 10 and 21, the combination of Aronson et al and Marmur teaches power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., see claim 6 of Aronson et al).

Regarding claims 11, 16-20 and 22-38, Similarly as described above, the combination of Aronson et al and Marmur teaches an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and transmitting the retimed and reshaped second serial electrical data stream (i.e., see claim 1 of Aronson et al and see Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 12, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 13, the combination of Aronson et al and Marmur teaches the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

This is a provisional obviousness-type double patenting rejection.

9. Claims 9 and 28 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-26 of Copending Application No. 10/629,302 (Aronson et al) in view of Marmur (US Patent No. 6,832,052) and further in view of Jiang et al (US Patent No. 6,665,498).

Regarding claims 9 and 28, the combination of Aronson et al and Marmur differs from claims 9 and 28 in that it fails to teach an adaptive equalizer. However, Jiang et al teaches an equalizer (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the equalizer as taught by Jiang et al in the system of the combination of Aronson et al and Marmur. One of ordinary skill in the art would have been motivated to do this since allowing reducing the distortion of the signal and reducing the noise signal and error signal.

This is a provisional obviousness-type double patenting rejection.

10. Claims 1-8, 10-27 and 29-43 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of copending Application No. 11/073,452 (Aronson et al). Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations recited in claims 1-8, 10-27 and 29-43 of the instant application are encompassed by claims 1-15 of copending Application No. 10/073,452 (Aronson et al).

10/629,301 (Claim 1)	Copending Application No. 11/073,452 (Claim 1)

An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream;	An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream (Claim 1);
receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;	receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream (Claim 1);
a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;	a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (Claim 1);
receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream;	receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (Claim 1);
a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;	a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit (Claim 1);
transmitter eye opener circuitry for	transmitter eye opener circuitry for

retiming and reshaping the second serial electrical data stream; and	retiming and reshaping the second serial electrical data stream (Claim 1); and
a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.	a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream (Claim 1).

Regarding claim 2, Aronson et al discloses wherein the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., see claims 1-15 of Aronson et al).

Regarding claim 3, Aronson et al discloses the receiver eye opener circuitry has a data rata range including 10 Gb/s; and the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s (i.e., see claims 1-15 of Aronson et al).

Regarding claim 4, Aronson et al discloses the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry (i.e., see claims 1-15 of Aronson et al).

Regarding claims 5-7, 14 and 15, Aronson et al discloses the bypass data path is selected in response to a loss of lock (LOL) signal or a loss of signal (LOS) signal or a

command received from external to the integrated circuit (i.e., see claims 1-15 of Aronson et al).

Regarding claims 8, Aronson et al discloses bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., see claims 1-15 of Aronson et al).

Regarding claims 10 and 21, Aronson et al discloses power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., see claims 1-15 of Aronson et al).

Regarding claims 11, 16-20 and 22-43, Similarly as described above, Aronson et al discloses an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and transmitting the retimed and reshaped second serial electrical data stream (i.e., see claims 1-15 of Aronson et al).

Regarding claim 12, Aronson et al discloses the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., see claims 1-15 of Aronson et al).

Regarding claim 13, Aronson et al discloses the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping (i.e., see claims 1-15 of Aronson et al).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

11. Claims 9 and 28 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of copending Application No. 11/073,452 (Aronson et al) in view of Jiang et al (US Patent No. 6,665,498).

Regarding claims 9 and 28, Aronson et al differs from claims 9 and 28 in that he fails to teach an adaptive equalizer. However, Jiang et al teaches an equalizer (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the equalizer as taught by Jiang et al in the system of Aronson et

al. One of ordinary skill in the art would have been motivated to do this since allowing reducing the distortion of the signal and reducing the noise signal and error signal.

This is a provisional obviousness-type double patenting rejection.

12. Claims 1-43 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 11/118,172 (Aronson et al). Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations recited in claims 1-43 of the instant application are encompassed by claims 1-18 of copending Application No. 11/118,172 (Aronson et al).

10/629,301 (Claim 1)	Copending Application No. 11/118,172 (Claims 1 and 2)
An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream;	An integrated circuit for use in a transceiver module, the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream (Claims 1 and 2);
receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;	receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream (Claims 1 and 2);
a first electrical output port for transmitting the retimed and reshaped first	a first electrical output port for transmitting the retimed and reshaped first

serial electrical data stream to external to the integrated circuit;	serial electrical data stream to external to the integrated circuit (Claims 1 and 2);
receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream;	receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (Claims 1 and 2);
a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;	a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit (Claims 1 and 2);
transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and	transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream (Claims 1 and 2); and
a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.	a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream (Claims 1 and 2).

Regarding claim 2, Aronson et al discloses wherein the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., see claims 1-18 of Aronson et al).

Regarding claim 3, Aronson et al discloses the receiver eye opener circuitry has a data rata range including 10 Gb/s; and the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s (i.e., see claims 1-18 of Aronson et al).

Regarding claim 4, Aronson et al discloses the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry (i.e., see claims 1-18 of Aronson et al).

Regarding claims 5-7, 14 and 15, Aronson et al discloses the bypass data path is selected in response to a loss of lock (LOL) signal or a loss of signal (LOS) signal or a command received from external to the integrated circuit (i.e., see claims 1-18 of Aronson et al).

Regarding claims 8, Aronson et al discloses bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., see claims 1-18 of Aronson et al).

Regarding claims 9 and 28, Aronson et al differs from claims 9 and 28 in that he fails to teach an adaptive equalizer (see claims 1-18 of Aronson et al).

Regarding claims 10 and 21, Aronson et al discloses power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., see claims 1-18 of Aronson et al).

Regarding claims 11, 16-20 and 22-43, Similarly as described above, Aronson et al discloses an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and transmitting the retimed and reshaped second serial electrical data stream (i.e., see claims 1-18 of Aronson et al).

Regarding claim 12, Aronson et al discloses the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., see claims 1-18 of Aronson et al).

Regarding claim 13, Aronson et al discloses the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping (i.e., see claims 1-18 of Aronson et al).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al (US Patent No. 6,665,498) in view of Marmur (US Patent No. 6,832,052).

Regarding claims 1, 11, 16, 17, 22-24 and 34, referring to Figure 2, Jiang et al teaches an integrated circuit (i.e., ASIC 212 in a transceiver) for use in a transceiver module, the integrated circuit (ASIC 212) comprising:

a first electrical input port for receiving a first serial electrical data stream (i.e., an electrical input port receiving a serial electrical data stream from photodiode 216, Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48);

receiver eye opener circuitry (i.e., ASIC 212, Fig. 2) for retiming and reshaping the first serial electrical data stream (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48);

a first electrical output port (i.e., the ASIC 212 having a electrical output port, Fig. 2) for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48);

a second electrical input port (i.e., ASIC 212 having a second electrical input port, Fig. 2) for receiving a second serial electrical data stream from external to the integrated circuit (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48);

transmitter eye opener circuitry (i.e., ASIC 212) for retiming and reshaping the second serial electrical data stream (i.e., Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48); and

a second electrical output port (the ASIC 212 having a second output port) for transmitting the retimed and reshaped second serial electrical data stream (Fig. 2, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48).

Jiang et al differs from claims 1, 11, 16, 17, 22-24 and 34 in that he does not specifically teach a receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream. However, Marmur teaches a receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (i.e., Figures 1 and 2, col. 2, lines 45-67 and col. 3, lines 1-46). Based on this teaching, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input

port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream as taught by Marmur in the system of Jiang et al. One of ordinary skill in the art would have been motivated to do this since allowing performance monitoring of optical signals of different transmission protocols at one or more different bit rates.

Regarding claims 2 and 12, the combination of Jiang et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 3 and 13, the combination of Jiang et al and Marmur teaches the receiver eye opener circuitry has a data rata range including 10 Gb/s; and
the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 4 and 18-20, the combination of Jiang et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 5-7, 14 and 15, the combination of Jiang et al and Marmur teaches the bypass data path is selected in response to a loss of lock (LOL) signal or a loss of signal (LOS) signal or a command received from external to the integrated circuit (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 8, the combination of Jiang et al and Marmur teaches bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 9 and 28, the combination of Jiang et al and Marmur teaches an equalizer (Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48).

Regarding claims 10 and 21, the combination of Jiang et al and Marmur teaches power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 25 and 35-38, the combination of Jiang et al and Marmur teaches the transceiver module is substantially compliant with the XFP MSA (i.e., Fig. 2 of Jiang et al).

Regarding claim 26, the combination of Jiang et al and Marmur teaches bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs at a data rate of about 8.5Gb/s (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 27, the combination of Jiang et al and marmur teaches at least one of the receive path bypass circuitry and the transmit path bypass circuitry comprises: a CDR; and a retimer (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4,

lines 1-67 and col. 5, lines 1-48 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 28, the combination of Jiang et al and Marmur teaches at least one of the receive path bypass circuitry and the transmit path bypass circuitry comprises one of: a passive equalization circuit; and an active equalization circuit (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 29, the combination of Jiang et al and Marmur teaches the transmit path eye opener circuitry and the receive path eye opener circuitry are data rate responsive (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 30, the combination of Jiang et al and Marmur teaches bypass of the receive path eye opener circuitry and transmit path eye opener circuitry can be implemented in at least one of the following ways: manually; and, automatically (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 31, the combination of Jiang et al and Marmur teaches bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs for a range of data rates less than about 10Gb/s (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 32, the combination of Jiang et al and Marmur teaches the receive path eye opener circuitry and receive path bypass circuitry collectively comprise

a receiver eye opener IC; and the transmit path eye opener circuitry and transmit path bypass circuitry collectively comprise a transmitter eye opener IC (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 33, the combination of Jiang et al and Marmur teaches the receiver eye opener IC and transmitter eye opener IC each comprise circuitry for a plurality of eye openers, each of the plurality of eye openers being configured to operate in connection with a predetermined data rate or predetermined range of data rates (i.e., Fig. 2 of Jiang et al, col. 3, lines 34-67, col. 4, lines 1-67 and col. 5, lines 1-48 Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

14. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wall et al (US Patent No. 7,308,060) in view of Marmur (US Patent No. 6,832,052).

Regarding claims 1, 11, 16, 17, 22-24 and 34, referring to Figures 1 and 2, Wall et al teaches an integrated circuit (i.e., receiver eye opener 32 and transmitter eye opener 20, Fig. 1) for use in a transceiver module, the integrated circuit comprising:

a first electrical input port (i.e., receiving eye opener 32 having a input port receiving a serial electrical data stream from photodiode 26, Fig. 1) for receiving a first serial electrical data stream (i.e., Figs. 1 and 2, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22);

receiver eye opener circuitry (i.e., receiver eye opener 32, Fig. 1) for retiming and reshaping the first serial electrical data stream (i.e., Figs. 1 and 2, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22);

a first electrical output port (i.e., the receiver eye opener 32 having a electrical output port, Fig. 1) for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (i.e., Figs. 1 and 2, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22);

a second electrical input port (i.e., the transmitter eye opener 20 having a second electrical input port, Fig. 1) for receiving a second serial electrical data stream from external to the integrated circuit (i.e., Figs 1 and. 2, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22);

transmitter eye opener circuitry (i.e., transmitter eye opener 20, Fig. 1) for retiming and reshaping the second serial electrical data stream (i.e., Figs. 1 and 2, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22); and

a second electrical output port (the transmitter eye opener 20 having a second output port, Fig. 1) for transmitting the retimed and reshaped second serial electrical data stream (i.e., Figs. 1 and 2, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22).

Wall et al differs from claims 1, 11, 16, 17, 22-24 and 34 in that he does not specifically teach a receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream. However, Marmur teaches a receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream (i.e., Figures 1 and 2, col. 2, lines 45-67 and col. 3, lines 1-46). Based on this teaching, it would have been obvious to one

having skill in the art at the time the invention was made to incorporate the receiver bypass circuitry for switchably selecting a bypass data path from the first electrical input port to the first electrical output port but bypassing retiming and reshaping of the first serial electrical data stream as taught by Marmur in the system of Wall et al. One of ordinary skill in the art would have been motivated to do this since allowing performance monitoring of optical signals of different transmission protocols at one or more different bit rates.

Regarding claims 2 and 12, the combination of Wall et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 3 and 13, the combination of Wall et al and Marmur teaches the receiver eye opener circuitry has a data rata range including 10 Gb/s; and the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 4 and 18-20, the combination of Wall et al and Marmur teaches the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 5-7, 14 and 15, the combination of Wall et al and Marmur teaches the bypass data path is selected in response to a loss of lock (LOL) signal or a

loss of signal (LOS) signal or a command received from external to the integrated circuit (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 8, the combination of Wall et al and Marmur teaches bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 9 and 28, the combination of Wall et al and Marmur teaches an equalizer (Figs. 1 and 2 of Wall et al, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22).

Regarding claims 10 and 21, the combination of Wall et al and Marmur teaches power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected (i.e., Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claims 25 and 35-38, the combination of Wall et al and Marmur teaches the transceiver module is substantially compliant with the XFP MSA (i.e., Figs. 1 and 2 of Wall et al).

Regarding claim 26, the combination of Wall et al and Marmur teaches bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs at a data rate of about 8.5Gb/s (i.e., Figs 1 and. 2 of Wall et al, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 27, the combination of Wall et al and Marmur teaches at least one of the receive path bypass circuitry and the transmit path bypass circuitry

comprises: a CDR; and a retimer (i.e., Figs 1 and 2 of Wall et al, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 28, the combination of Wall et al and Marmur teaches at least one of the receive path bypass circuitry and the transmit path bypass circuitry comprises one of: a passive equalization circuit; and an active equalization circuit (i.e., Figs. 1 and 2 of Wall et al, col. 5, lines 26-67, col. 6, lines 1-67 and col. 7, lines 1-22 and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 29, the combination of Wall et al and Marmur teaches the transmit path eye opener circuitry and the receive path eye opener circuitry are data rate responsive (i.e., Figs. 1 and 2 of Wall et al and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 30, the combination of Wall et al and Marmur teaches bypass of the receive path eye opener circuitry and transmit path eye opener circuitry can be implemented in at least one of the following ways: manually; and, automatically (i.e., Figs. 1 and 2 of Wall et al and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 31, the combination of Wall et al and Marmur teaches bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs for a range of data rates less than about 10Gb/s (i.e., Figs. 1 and 2 of Wall et al and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 32, Wall et al and Marmur teaches the receive path eye opener circuitry and receive path bypass circuitry collectively comprise a receiver eye opener

IC; and the transmit path eye opener circuitry and transmit path bypass circuitry collectively comprise a transmitter eye opener IC (i.e., Figs. 1 and 2 of Wall et al and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Regarding claim 33, the combination of Wall et al and Marmur teaches the receiver eye opener IC and transmitter eye opener IC each comprise circuitry for a plurality of eye openers, each of the plurality of eye openers being configured to operate in connection with a predetermined data rate or predetermined range of data rates (i.e., Figs. 1 and 2 of Wall et al and Figures 1 and 2 of Marmur, col. 2, lines 45-67 and col. 3, lines 1-46).

Allowable Subject Matter

15. Claims 39-43 are allowed (if overcome the double patenting rejection).

Response to Arguments

16. Applicant's arguments with respect to claims 1-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh Phan whose telephone number is (571)272-3035.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

/Hanh Phan/

Primary Examiner, Art Unit 2613